**WE CLAIM:**

1. A display, comprising:

a chamber to store a volume of liquid crystal material, the chamber having a viewable region and a non-viewable region, and

at least one polymer memory cell provided in a non-viewable region of the chamber.

2. The display of claim 1, further comprising a pixel transistor also located in the non-viewable region of the chamber, and separate sets of control lines for each of the polymer memory cell and the pixel transistor.

3. The display of claim 2, wherein the control lines are provided in one or more stack of control lines to reduce a profile of the control lines when considered from a viewable area of the display.

4. The display of claim 1, further comprising a backlight provided on an exterior surface of the display.

5. The display of claim 1, further comprising a reflector provided on an exterior surface of the display.

6. The display of claim 1, further comprising an opaque filter coincident with the non-viewable region of the display.

7. A display comprising:

a chamber to store liquid crystal material,

a plurality of display transistors arranged in an array across a planar surface of the chamber, the display transistors to define pixels of the display,

a memory system having polymer memory cells provided within the liquid crystal chambers.

8. The display of claim 7, wherein the chamber includes viewable and non-viewable regions and the memory cells are co-located with a non-viewable region thereof.

9. The display of claim 7, wherein polymer memory cells are co-located with the display transistors.

10. The display of claim 7, wherein the polymer memory system comprises:

a plurality of memory cells,

a driving line coupled to each of the cells, and

a plurality of data lines, one coupled to each of the cells.

11. The display of claim 7, wherein the polymer memory system comprises a plurality of layers, each layer comprising:

a plurality of memory cells,

a driving line coupled to each of the cells in the respective layer, and

a plurality of data lines, one coupled to each of the cells in the respective layer.

12. The display of claim 7, further comprising a backlight coupled to one surface of the display.

13. The display of claim 7, further comprising a reflector coupled to one surface of the display.

14. The display of claim 7, wherein each chamber comprises:

liquid crystal material provided within the chamber,

a pixel transistor coupled to a first control line on a first surface of the chamber, and

a second control line provided on a second surface opposite the first surface.

15. A computer system comprising: a processor, a memory system and an LCD display, each coupled together via a communication fabric, wherein the memory system includes polymer memory cells distributed among LCD materials of the display.

16. The system of claim 15, wherein the memory system comprises:

a plurality of polymer memory cells,

a driving line coupled to each of the polymer memory cells, and

a plurality of data lines, one coupled to each of the polymer memory cells.

17. The system of claim 15, wherein the memory system comprises a plurality of layers, each layer comprising:

a plurality of polymer memory cells,

a driving line coupled to each of the polymer memory cells in the respective layer, and

a plurality of data lines, one coupled to each of the polymer memory cells in the respective layer.

18. A method, comprising addressing a display system and reading data therefrom.

19. The method of claim 18, further comprising addressing the display system providing graphics data to the display.

20. The method of claim 19, wherein addressing of a memory cell within a display is staggered in time from addressing of a co-located pixel of the display.